CLAIMS:

1. Circuit comprising

- a noise suppressing circuitry (40; 69) having an input (42; 70) for a first voltage (VDD) and an output (43; 68) for providing a supply voltage (VDDfiltered),
- a MOSFET-based switch (41) with a MOSFET (MP) being situated in a well (67), where a supply voltage (VDDfiltered) can be applied to well (67),

whereby

- the first voltage (VDD) is a global voltage used elsewhere in the same circuit,
- the supply voltage (VDDfiltered) is less-noisy than the first voltage (VDD), and
- the noise suppressing circuitry (40; 69) has a noise suppression characteristic where frequencies within a bandwidth range around the upper edge of the circuit's frequency band are damped.

2. The circuit of claim 1, whereby the MOSFET is a P-MOSFET (MP) and the well is an n-well (67).

3. The circuit of claim 1 or 2, whereby the noise suppressing circuitry is a filter (40; 69), preferably a low-pass filter or a band-pass filter.

4. The circuit of claim 1 or 2, whereby the noise suppressing circuitry is a voltage regulator and the supply voltage (VDDfiltered) is smaller than the first voltage (VDD).

5. The circuit of claim 3, whereby the filter (40; 69) is a 1st-order filter.

6. The circuit of claim 5, whereby the filter (40) comprises pMOS transistors (MP0, MP1), a current source (Ib) and at least one capacitor (C).

7. The circuit of claim 3 or 6, whereby the filter (40) comprises simulated resistors, preferably resistors being simulated by two pMOS transistors (MP0, MP1).

8. The circuit of one of the preceding claims, whereby the n-well (67) has the highest potential of the whole circuit.

9. The circuit of one of the preceding claims being an analog circuit or a mixed-signal circuit.

10. Automatic gain control (AGC) comprising a circuit according to one of the preceding claims.